Development of Quantum Well Thermoelectric Device

(From 18th Int. Conf. On Thermoelectrics, Proceeding, ICT'99)

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Abstract

The electronic and thermal properties of bulk materials are altered when they are incorporated into quantum wells. Two-dimensional quantum wells have been synthesized by alternating layers of B_4C and B_9C in one system and alternating layers of Si and $Si_{0.8}Ge_{0.2}$ in another system. Such nanostructures are being investigated as candidate thermoelectric materials for high figures of merit (Z). The predicted enhancement is attributed to the confined motion of charge carriers and phonons in the two dimensions and separating them from the ion scattering centers.

Molecular beam epitaxy (MBE) and sputtering techniques have been used to prepare these multilayer films. Films have been deposited on single-crystal silicon substrates. The " and D properties of these films have been determined over a broad range of temperatures from 4.2K to l200K and were previously reported. The "^{2}/D values for these P type B-C and N type SiGe films were more than a factor of 10 to 30 times higher than bulk P type B-C and N type SiGe.

Several one and two couple devices were fabricated with P-type B_4C/B_9C QW films and N-type bulk Bi_2Te_3. One of these couples produced 0.182 milliwatt at a) T of a 50/C. This device produced ten times more power than the bulk Bi_2Te_3 commercial material of the same dimensions and) T. Hi-Z is also producing thicker B_4C/B_9C films (>10 :m) on thinner Si substrates (<1 :m) to minimize thermal bypass heat losses. Successful scale up of these films for the P-leg is expected to yield a 1 cm square device that will produce ~5 Watts at a) T of 200/C. With a minimum assumption for thermal losses the device efficiency should approach 20%.

Background

Thermoelectric materials are utilized for power generation in remote locations, on spacecraft used for interplanetary exploration, and in places where waste heat can be recovered. Broader usage is limited by the efficiency of present systems and the power-specific cost ($/W) of power generation. Materials with a ZT$6 can lead to a factor of 2 to 3 improvement in thermodynamic efficiency. Recall that the thermodynamic efficiency, 0, of a thermoelectric power generator is

$$\eta = \frac{T_h - T_c}{T_h}\left[\frac{M - 1}{M + T_c/T_h}\right] \qquad (1)$$

where M is defined as

$$M = \sqrt{1 + \frac{1}{2}\,\bar{Z}\,(T_c + T_h)} \qquad (2)$$

and T_h is the absolute temperature at the hot junction and T_c is the absolute temperature at the cold junction. To achieve a high efficiency with a power generator, the overall figure of merit for the device, *Z*, must be high. The figures of merit of the thermoelectric materials used to construct the device must also be high. For a specific material, *Z* is defined as:

$$Z = \frac{\sigma\alpha^2}{\kappa_{ph} + \kappa_{el}} \qquad (3)$$

where F is the electrical conductivity, " is the Seebeck coefficient, 6_{ph} is the phonon contribution to the thermal conductivity, and 6_{el} is the electronic contribution to the thermal conductivity. Note that 6_{ph} is also known as 6_L, the lattice thermal conductivity. Much of the effort to improve Z over the past 20-30 years has focused on attempts to reduce 6_L without adversely affecting the electrical conductivity. Some success has been achieved with solid-solution alloying. Further reductions in 6_L have been achieved by reducing the grain size of silicon-germanium alloys, however, this approach is still in its infancy and the potential benefit is believed to be relatively small.

Multilayer films of B_4C/B_9C and $Si/Si_{0.8}Ge_{0.2}$ are being investigated as a means of achieving a high Z. Models based upon quantum mechanics predict that such structures should have an unusually high Z [1-5]. The quantum-well (QW) layer is sandwiched between two barrier layers. Typically, the QW material has a very narrow band gap and the barrier material has a relatively large band gap. Molecular beam epitaxy (MBE) and sputtering have been employed to fabricate the samples.

For power applications, the concern is that the above materials will inter-diffuse at some elevated temperature and lose their two-dimension structure and associated quantum well properties. For power generation applications, B-C and SiGe alloys appeared to be the best initial selection for the following reasons:

C B-C have very low diffusion coefficients in one another.
C Si and Ge have very low diffusion coefficients in one another. The dopants boron and phosphorous however can diffuse much quicker and high temperature aging studies will be necessary to determine how long these films will remain stable at the anticipated operating temperatures.
C B-C as well as SiGe alloys do not have to be deposited in

an exact stoichiometry to be useful thermoelectric materials.

C Since stoichiometry is not critical, the deposition process can be conducted with less critical controls.

Experimental

" and D Measurements

Room temperature resistivities were measured on samples using the following method: the current was introduced at the ends of a long, rectangular cut sample and the voltage probes were near the center of the test specimen. The resistance was obtained from the voltage drop, and the resistivity was calculated by knowing the cross-sectional area of the bar and the distance between the two voltage probes (ASTM F-43). The Allesi instrument, which uses pressure contacts, was used as the voltage probes in this case.

The high temperature " and D of the films were measured in a system at Hi-Z and the results have been published previously [4, 5]. The electrical resistivities of the samples were measured as a function of temperature from 300K to 1200K using a Linear Research LR400 4-wire bridge operating at 16Hz. Electrical contact to the films was made by wrapping nickel wire around the sample, and bonding the wires to the surface with silver paint. The thermocouple leads were held to the surface of the sample with the nickel wires, and bonded in place with the silver paint. Currents for the measurements were in the range of 1 to 100 mA.

N and P Couple

Several B_4C/B_9C-Bi_2Te_3 and B_4C/B_9C-Si/SiGe P-N couples (shown in Figure 1) with low contact resistance were fabricated and the results appear very promising. Each leg in a couple consist of a square of 1000D thick multilayer of B_4C/B_9C (P type) and Si/SiGe (N type) films. The films are deposited on 0.5 mm thick silicon substrate that is approximately 1cm×1cm. At a)T . 50/C (T_{cold} . 40/C and T_{hot} . 90/C), the voltage measured on this couple was ~ 0.1 Volts. The contact resistance was a few ohms which was very low compared to the total resistance of the couple which was approximately 20 kS. This is the resistance of the films and does not include the Si substrate [4, 5]. The results

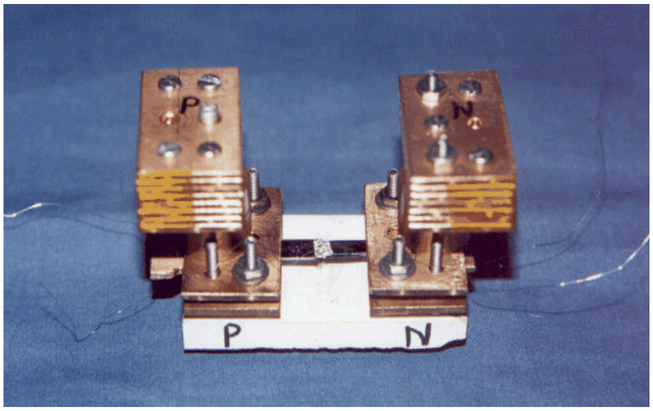

Figure 1. Schematic of P-N couple test fixture.

Table 1. Device performance.

Performance of MLQW Couples.		Matched Load Power (µW)	Efficiency (%) T_{cold} . 40°C and T_{hot} . 90°C	Calculated Efficiency (%) T_{cold} . 50°C and T_{hot} . 250°C
1	B_4C/B_9C-Si/SiGe P-N Single Couple on 0.5mm Si	0.120	**~4.4** if bulk $\kappa_{thermal}$ is assumed and **~11** if newly measured $\kappa_{thermal}$ is assumed	**~11** if bulk $\kappa_{thermal}$ is assumed and ~**24** if newly measured $\kappa_{thermal}$ is assumed
2	B_4C/B_9C-Bi_2Te_3 P-N Single Couple Device on 0.5mm Si	0.090	**~4** if bulk $\kappa_{thermal}$ is assumed and ~**10** if newly measured $\kappa_{thermal}$ is assumed	**~10** if bulk $\kappa_{thermal}$ is assumed and **~22** if newly measured $\kappa_{thermal}$ is assumed
3	B_4C/B_9C-Bi_2Te_3 P-N Two Couples Device on 0.5 mm Si	0.182	**~4** if bulk $\kappa_{thermal}$ is assumed and **10** if newly measured $\kappa_{thermal}$ is assumed	**~10** if bulk $\kappa_{thermal}$ is assumed and **~22** if newly measured $\kappa_{thermal}$ is assumed
4	B_4C/B_9C-Bi_2Te_3 P-N Single Couple on 7µm Si	0.105	**~6** if bulk $\kappa_{thermal}$ is assumed and ~**12** if newly measured $\kappa_{thermal}$ is assumed	**~15** if bulk $\kappa_{thermal}$ is assumed and **~26** if newly measured $\kappa_{thermal}$ is assumed
5	Bulk Bi_2Te_3-Bi_2Te_3 Device	0.01	3	7
6	Bulk B_9C-Bi_2Te_3 Device	.005	>1	>1

are tabulated in the Table 1. Efficiency was obtained as follows: {i} Power data, " and D, were measured at a T_{hot} = 90/C and T_{cold} = 40/C. {ii} The Z for the couple, over the) T = 90/C - 40/C, was calculated using bulk thermal 6 property data. {iii} Efficiency was then calculated using the formulas 1 through 3.

These values of voltage and resistance give a matched load power of about 0.125 : W (micro-Watts) for the couple at a T_{cold} . 40/C and T_{hot} . 90/C. At these same temperatures and dimensions a bulk Bi_2Te_3 couple produces only 0.01 : W, a bulk B_9C-SiGe couple produces only 0.004 : W, and a bulk SiGe couple produces 0.02 : W. Therefore the B_4C/B_9C-Si/SiGe P-N couple produces about ten times more power, than the bulk BiTe couple and about thirty times more power than bulk B_9C-SiGe couple. Although this couple was fabricated with thin films (only 1000D), Hi-Z hopes to duplicate these results with much thicker films (100,000D) on a thinner or insulating substrate. Silicon substrates with thicknesses of 5 : m (micro-meter) and 10 : m are available commercially as are insulating substrates like Kapton. If fabrication of thick films on these substrates is successful then a 1cm×1cm couple, like the one described above, would produce 1250 : W of power at a) T . 50/C. The final goal is to fabricate and measure the properties of these thicker P-N couples on very thin or insulating substrates.

Results & discussion

Evaluation of Samples and Substrate Correction

In the case of the heterostructures the measurement of thermoelectric properties were complicated by the conductivity of the substrate. In this particular case, most of the films were deposited on standard 10S-cm Si (100). The relatively high conductivity of this substrate has made it necessary to correct the result to eliminate substrate contributions to the electrical conductivity, F, and the Seebeck coefficient, ". the measured resistance R_{total}, consists of the resistance of the film, R_{films}, and the resistance of the substrate, $R_{substrate}$,

$$\frac{1}{R_{total}} = \frac{1}{R_{substrate}} + \frac{1}{R_{film}} \qquad (4)$$

By making independent measurements of the substrate resistance, the film resistance can be calculated from the measured value,

$$R_{film} = \frac{1}{\frac{1}{R_{total}} - \frac{1}{R_{substrate}}} \qquad (5)$$

Given the dimensions of the film the actual conductivity of the hetrostructure can then be calculated directly,

$$\sigma_{films} = \frac{1}{\rho_{films}} = \left(\frac{L}{WH}\right)\frac{1}{R_{films}} \qquad (6)$$

Similar corrections must be made in cases involving measurements of the Seebeck coefficient. The substrate and film are treated as two parallel branches of a linear circuit, each composed of a (thermal) battery and a resistor.

The measured thermoelectric voltage of the film, V_{film}, can be expressed in term of the measured voltage, V_{total}, the known voltage of a bare substrate, $V_{substrate}$, the resistance of the film, R_{film}, and the resistance of the bare substrate, $R_{substrate}$,

$$V_{film} = \left(1 + \frac{R_{film}}{R_{substrate}}\right)V_{total} - \left(\frac{R_{film}}{R_{substrate}}\right)V_{substrate} \qquad (7)$$

The Seebeck coefficient is then,

$$\sigma_{film} = \frac{V_{film}}{T_h - T_c} \qquad (8)$$

Obviously, when measuring the Seebeck of thin films, it is important to minimize the substrate contribution to the extent possible by making the ration $R_{film}/R_{substrate}$ as small as possible. Al_2O_3 is an ideal substrate for electronic measurements of thin films since no correction of the Seebeck coefficient is required for such insulating materials. In the case of 1000 S-cm float-zone Si (100) substrates, the uncompensated error in the measured Seebeck coefficient is on the order of 1%. In the case of 10 S-cm Si (100), the possible error introduced by the substrate can be much larger and must be accounted for.

Thermal and Electrical Loss Due to Si Substrate

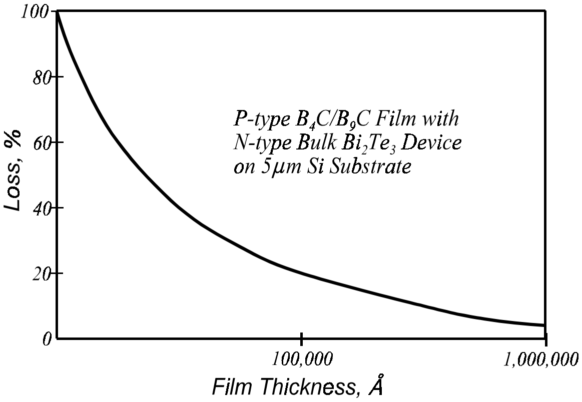

Figure 2. Thermal and Electrical Loss for QW Device on Si Substrate.

Total electrical and thermal loss of 5 : m thick Si substrate with and film thickness of 10 : m will be about 20% as it is shown in Figure 2. And the loss at 30 : m film thickness is only 10%. 10 : m film on 0.5mm Si substrates could routinely be fabricated. Similar films could also be fabricated on 5 : m Si.

A one watt QW device could be fabricated from these films

Table 2. Fabrication of one Watt Quantum Well (QW) Module

Film Thickness	Film Fabrication	Number of Couples
~1000D	Routine deposition	~166,250
~100,000D (~0.0004")	Demonstrated many times	~1662
~300,000D	Demonstrated one time	~555
~1,000,000D (~0.004")	Possible, remain to be demonstrated	~166

with combinations shown in Table 2. With loss of less than 10 to 20%, QW devices similar to these could be the first generation of commercial QW device.

Acknowledgment

This program was sponsored by the Department of Defense (DOD) MURI program which Hi-Z is a subcontractor to UCLA with Dr. John Pazik the DOD Program Manager, and Department of Energy (DOE) under a Phase II SBIR grant with Dr. William Barnett the DOE Program Manager.

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